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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/826,198	04/15/2004	Symon Brewer	21-014	9819

22898 7590 10/05/2005

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EXAMINER	
WONG, LINDA	
ART UNIT	**PAPER NUMBER**
2634	

DATE MAILED: 10/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/826,198	BREWER, SYMON	
	Examiner	Art Unit	
	Linda Wong	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 April 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Arguments

Drawings

1. The drawings are objected to because written labels for components of the invention are needed to clarify the drawings. For example, label 218 should have a written term "Dither Unit" along with the numerical number.

   Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claims' Rejections and Objections

2. Applicant's arguments filed 7/25/2005 have been fully considered but they are not persuasive for **claims 1-2, 4**.

3. Regarding the arguments to **claim 1**, the applicant states in the argument the 35 USC 103 is not valid due to the single output from the variable delay line disclosed by Kelkar et al (Fig. 5) and dual input to the edge detector disclosed by Yanagisawa et al (Fig. 7). It is agreed that the variable delay line only outputs a single output but Kelkar et al discloses a phase detector that receives two inputs, one from the output of the variable delay line and the other the input signal. Thus, it would be obvious to

one skilled in the art to incorporate the variable delay line disclosed by Kelkar et al with the comparison pulse generator disclosed by Yanagisawa et al, wherein one of the inputs to the comparison pulse generator is the output from the variable delay line and the other input is the input signal as shown in Fig. 5 of Kelkar et al's invention to produce multiple delays of the input signal to make the jitter between the signals easily detectable. (Abstract of Yanagisawa et al, lines 2-3).

4. Regarding **claims 2,4,** the rejection still stands due to the rejection of the independent claim 1. Below are the rejections to claims 1-2,4, as disclosed in the previous office actions.
5. Regarding **claim 6**, the explanation for claim 1 refers to the validity of the rejection of claim 6. Also, Sunter et al also mentions measuring the peak to peak value of the interval where the jitter occurs in the signal on page 7, paragraph [0099], page 8, paragraph [0106], and page 9, paragraph [0110].
6. Regarding claims **7,9-10**, the rejection still stands due to the rejection of the independent claim 6. Below are the rejections to claims 6-10, as disclosed in the previous office action.
7. Regarding **claims 11 and 16**, the explanation for claim 1 refers to the validity of the rejection of claims 11 and 16. The rejection to claim 11 still stands as stated in the previous office action.
8. Regarding claims **12-15 and 17,19-20**, the rejection still stands due to the rejection of the independent claims 11 and 16. Below are the rejections to claims 6-10, as disclosed in the previous office action.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. **Claims 1, 4** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kelkar et al. (US Patent No.: 5663991) in view of Yanagisawa et al. (US Patent No.: 6528982).
   a. **Claim 1**, Kelkar et al discloses an inputting signal to generate signal transition locations (Fig. 5, labels 84 and 83), latching or sorting the transition location using a sampling clock signal (Col. 3, lines 42-44), converting the signal transition to a delay value (Col. 3, 45-53). Although Kelkar et al does not disclose converting the delay value to an edge position and detecting a value of the edge position, Yanagisawa et al discloses an edge detector converts the first and second signal into first and second timing signals, a comparison pulse generator that outputs the phase difference or delay value of the first and second timing signals. (Fig. 7, labels 107 and 103) It would be obvious to one skilled in the art to combine Kelkar et al's invention with Yanagisawa et al to produce multiple delays of the input signal to make the jitter between the signals easily detectable. (Abstract of Yanagisawa et al, lines 2-3)
   a. **Claim 4**, Yanagisawa et al discloses a comparator comparing the phase different or edge movement exceeding a predetermined value. (Abstract, lines 9-12)

2. **Claims 2, 6-7, 9-12, 14-15** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kelkar et al (US Patent No.: 5663991) in view of Yanagisawa et al. (US Patent No.: 6528982) and further in view of Sunter et al. (US Application No.: 20050069031).
   a. **Claim 2**, Although neither Kelkar et al nor Yanagisawa et al discloses a filter, Sunter et al. discloses a jitter reducing system comprising a filter after detecting a phase error and before the analysis circuit. (Fig. 6B, label filter) It would be obvious to one skilled in the art to include a filter in a system for reduction of jitter to filter out high frequencies. (Col. 15, lines 26-28)
   b. **Claim 6** inherits all the limitations of Claim 1. Although neither Kelkar et al and Yanagisawa et al discloses a peak-to-peak detection and output, Sunter et al discloses an analysis circuitry measuring and outputting the peak-to-peak value of the latched output data signal. (Fig. 3, label

22) It would be obvious to one skilled in the art to include an analysis circuitry to provide a "simpler, lower cost technique that accurately measures jitter." (Page 2, paragraph [0015])

c. **Claim 7** inherits all the limitations of claim 2.

d. **Claim 9** inherits all the limitations of claim 4.

e. **Claim 10** inherits all the limitations of claim 5.

f. **Claim 11**, Kelkar et al discloses a tapped delay line (Fig. 2, labels 33, 35, 37, 39), a sampling clock or a measured clock (Fig. 2, label 26), a sample register for latching the signal transitions. (Fig. 2, labels 36, 38, 40, 42) Although Kelkar et al does not teach a priority encoder, and converter, Yanagisawa et al discloses an encoder in the form of a comparator detecting the phase difference or delay value and a converter in the form of a periodic signal generator outputting a signal for each width or delay value or phase difference. (Fig. 1, labels 103, 104) It would be obvious to one skilled in the art to combine Kelkar et al's invention with Yanagisawa et al to produce multiple delays of the input signal to make the jitter between the signals easily detectable. (Abstract of Yanagisawa et al, lines 2-3) Although neither Kelkar et al nor Yanagisawa et al discloses a peak-to-peak detector, Sunter et al discloses an analysis circuit that calculates the peak-to-peak value of the latched signal. (Fig. 6A, label 22) It would be obvious to one skilled in the art to include an analysis circuitry to provide a "simpler, lower cost technique that accurately measures jitter." (Page 2, paragraph [0015])

g. **Claim 12** inherits all the limitations of claim 2.

h. **Claim 14** inherits all the limitations of claim 4.

i. **Claim 15** inherits all the limitations of claim 5.

3. **Claims 16-17, 19-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kelkar et al (US Patent No.: 5663991) in view of Yanagisawa et al. (US Patent No.: 6528982) further in view of Sunter et al. (US Application No.: 20050069031) and further in view of IEEE Design and Test of Computers, "FPGA and CPLD Architectures: A Tutorial".

a. **Claim 16** inherits all the limitations of claim 11. Although a field programmable gate array carry chain (FPGA carry chain) is not disclosed by Kelkar et al, Yanagisawa et al and Sunter et al, based on the tutorial provided by IEEE Design and Test of Computers, "FPGA and CPLD Architectures: A Tutorial", an FPGA is a programmable array of flip-flops or logic gates. Kelkar et al discloses a variable delay line, which is equivalent to an FPGA. (Fig. 5, label 83) It would be obvious to one skilled in the art to provide an FPGA carry chain comprised of a interchanging or programmable delay line to provide a more robust, dynamic array of logics to decrease cost and provide very high pin-to-pin speed performance. (Definitions: page 43 under Terminology, pg 43, Col. 3, line 4 and pg 44, Col. 1, lines 1-2)

b. **Claim 17** inherits all the limitations of claim 2.

c. **Claim 19** inherits all the limitations of claim 4.

d. **Claim 20** inherits all the limitations of claim 5.

9. Applicant's arguments, see Applicant's Arguments, filed 7/25/2005, with respect to the rejection(s) of claim(s) 5 under Sunter et al have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Kelkar et al (US Patent No.: 5663991) in view of Yanagisawa et al (US Patent No.: 6528982) and further in view of Jungerman et al (US Publication No.: 20040146097).

Claim Rejections - 35 USC § 103

10. **Claim 5** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kelkar et al (US Patent No.: 5663991) in view of Yanagisawa et al. (US Patent No.: 6528982) ,

further in view of Sunter et al (US Publication No.: 20050069031) and further in view of Jungerman et al. (US Application No.: 20040146097).

a. **Claim 5**, Although Kelkar et al and Yanagisawa et al does not disclose calculating the root mean square (RMS) of the edge position, Sunter et al discloses a measuring the RMS value of the jitter found within a time interval but Sunter et al does not disclose calculating the RMS value of the edge position. (page 7, paragraph 0097] Jungerman et al discloses a method of detecting jitter comprising calculating the RMS value of the slope of the designated edge corresponding to the random component of the jitter. (page 1, paragraph [0005] and Fig. 2) It would be obvious to one skilled in the art to measure the RMS value at the position of the edge as taught by Jungerman et al and incorporating such measurement to Sunter et al's invention to establish sources of the jitter and predict the bit error rate of the communication system so to effectively eliminate jitter found in the signal.

11. Applicant's arguments, see Applicant's Arguments, filed 7/25/2005, with respect to the rejection(s) of **claim(s) 3,8,13** under Suzuki have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Kelkar et al (US Patent No.: 5663991) in view of Yanagisawa et al (US Patent No.: 6528982) and further in view of Soma et al (US Patent No.: 6795496).

Claim Rejections - 35 USC § 103

12. **Claim 3** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kelkar et al (US Patent No.: 5663991) in view of Yanagisawa et al. (US Patent No.: 6528982) , further in view Soma et al (US Patent No.: 6795496).

    a. **Claim 3**, Although Kelkar et al and Yanagisawa et al does not disclose inserting dither or random timing delays into the input signal prior to detecting and eliminating jitter, Soma et al disclose a jitter measuring device, wherein the PLL under test inserts jitter or dither or random timing delays into the input signal prior to detecting and removing jitter. (Fig. 32, labels 17 and Col. 4, lines 34-67)

13. **Claims 8 and 13** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kelkar et al (US Patent No.: 5663991) in view of Yanagisawa et al. (US Patent No.: 6528982) , further in view of Sunter et al (US Publication No.: 20050069031) and further in view of Soma et al (US Patent No.: 6795496).

    a. **Claims 8 and 13** inherit all the limitations of claim 3.

14. **Claim 18** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kelkar et al (US Patent No.: 5663991) in view of Yanagisawa et al. (US Patent No.: 6528982), further in view of Sunter et al (US Publication No.: 20050069031), further in view of IEEE Design and Test of Computers, "FPGA and CPLD Architectures: A Tutorial" and further in view of Soma et al (US Patent No.: 6795496).

    a. **Claim 18** inherits all the limitations of claim 3.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

    a. Yamaguchi et al (US Publication No.: 20040062301)

    b. Rao (US Publication No.: 20040131113)

    c. Yamaguichi et al (US Publication No.: 20050031029)

    d. Dalal et al (US Patent No.: 6661836)

    e. Dodds et al (US Publication No.: 20020031113).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linda Wong whose telephone number is 571-272-6044. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (571) 272-3056. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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